## LISTING OF CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A program development support apparatus comprising:

a CPU (Central Processing Unit) for executing a target program and outputting instruction address/instruction code data;

event management means for asserting and outputting a section trace start signal upon detecting that the instruction address/instruction code data from said CPU matches at least one of a predetermined instruction address and a predetermined instruction code set as an event condition in advance, the predetermined instruction code being different from a branch instruction;

trace data generation means for;

outputting an uncompressed instruction address as trace data when an instruction code of the instruction address/instruction code data from said CPU is a branch instruction;

outputting the uncompressed instruction address as the trace data when the section trace start signal from said event management means is active;

generating a plurality of compressed instruction addresses by compressing the instruction address of the instruction address/instruction code data, combining the compressed instruction addresses, and outputting the compressed instruction addresses as the trace data when the instruction address of the instruction address/instruction code data is not a branch instruction and the section trace start signal is not active; and

a trace memory for storing the trace data from said trace data generation means.

2. (Previously Presented) The apparatus according to claim 1, wherein said event management means keeps a data latch signal active during a predetermined period and outputting the data latch signal; and said trace data generation means receives the instruction address/instruction code data from said CPU and the section trace start signal from said event management means and, when the data latch signal from said event management means is active, latches the instruction address/instruction code data

3. (Previously Presented) The apparatus according to claim 2, wherein said event management circuit means comprises:

event setting means in which event setting data containing the predetermined instruction address/instruction code as the event condition and the active period of the data latch signal are set in advance; and

event detection means for, upon detecting that the instruction address/instruction code contained in the event setting data output from said event setting means matches the instruction address/instruction code of the instruction address/instruction code data from said CPU, asserting and outputting the section trace start signal and asserting the data latch signal during the active period set in said event setting means and outputting the data latch signal.

4. (Previously Presented) The apparatus according to claim 2, wherein said trace data generation means comprises:

instruction address/instruction code latch means for latching the instruction address/instruction code data from said CPU during the active period of the data latch signal and outputting the instruction address/instruction code;

instruction address data compression means for, when a received uncompressed data selection signal is active, outputting the instruction address from said instruction address/instruction code latch means as the compressed instruction address, and when the uncompressed data selection signal is not active, outputting difference data obtained by subtracting an immediately preceding instruction address from a current instruction address as the compressed instruction address;

branch instruction determination means for determining whether the instruction code from said instruction address/instruction code latch means is the branch instruction, and upon determining that the instruction code is the branch instruction, asserting and outputting a branch instruction detection signal;

trace control means for, when the received uncompressed data selection signal is active, outputting the compressed instruction address from said instruction address data compression means as trace data, and when the uncompressed data selection signal is not active, combining a plurality of continuously received compressed instruction addresses in accordance with a bit width of said trace memory and outputting the combined instruction addresses as the trace data, and outputting a trace data write signal for instructing said trace memory to write the trace data and a trace memory address for designating a storage address of said trace memory; and,

OR means for asserting and outputting the uncompressed data selection signal when at least one of the branch instruction detection signal from said branch instruction determination means and the section trace start signal from said event management means is active.

5. (Previously Presented) The apparatus according to claim 4, wherein said apparatus further comprises:

frame address comparison means for asserting and outputting a frame match signal when the instruction address/instruction code contained in the event setting data output from said event setting means matches the trace memory address from said trace control means; and,

said OR means asserting and outputting the uncompressed data selection signal when at least one of the branch instruction detection signal from said branch instruction determination means, the section trace start signal from said event detection means, and the frame match signal from said frame address comparison means is active.

6. (Canceled).